TDK SEMICONDUCTOR CORP.

78Q2120-64CGT
10/100BASE-TX
Ethernet Transceiver

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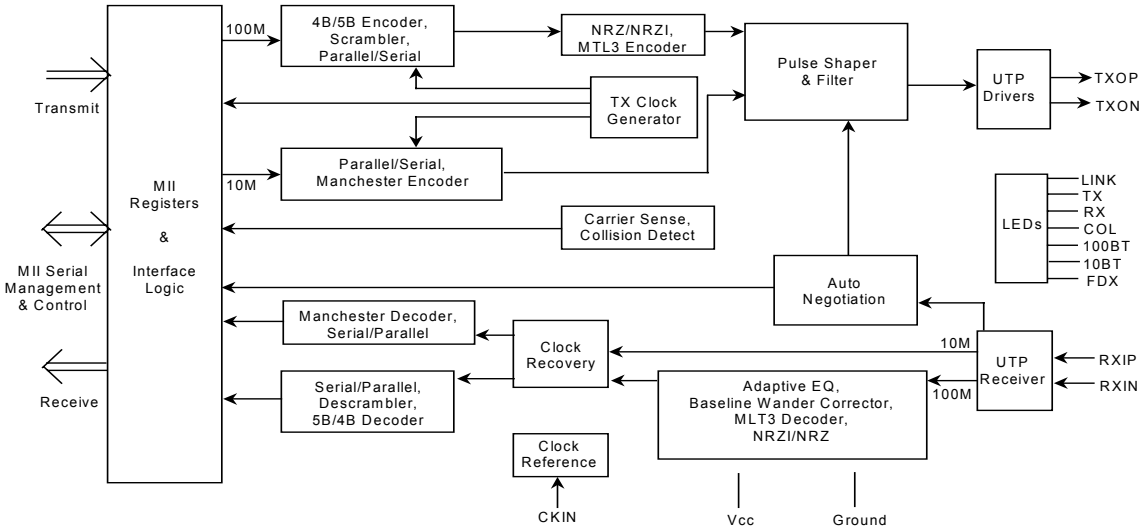
DESCRIPTION

The 78Q2120-64CGT is a 10BASE-T/100BASE-TX Fast Ethernet transceiver. It includes integrated MII, ENDECs, scrambler/descrambler, dual-speed clock recovery, and full-featured auto-negotiation functions. The transmitter includes an on-chip pulse-shaper and a low-power line driver. The receiver has an adaptive equalizer and a baseline restoration circuit required for accurate clock and data recovery. The transceiver interfaces to Category-5 unshielded twisted pair (Cat-5 UTP) cabling for 100BASE-TX/10BASE-T and Category-3 unshielded twisted pair for 10BASE-T, and is connected to the line media via 1:1 isolation transformers. No external filter is required. Interface to the MAC is accomplished through an IEEE-802.3 compliant media independent interface (MII). The product is fabricated in a BiCMOS process for high performance and low power operation.

FEATURES

- **10BASE-T/100BASE-TX IEEE-802.3 compliant TX and RX functions requiring a dual 1:1 isolation transformer interface to the line**
- **Integrated MII, 10BASE-T/100BASE-TX ENDEC, 100BASE-TX scrambler/descrambler, and full-featured auto-negotiation function**
- **Full duplex operation capable**
- **PCS Bypass supports 5-bit symbol interface**
- **Dual speed clock recovery**
- **Automatic polarity correction during auto-negotiation and 10BASE-T signal reception**
- **Power-saving and power-down modes including transmitter disable**
- **LED indicators: LINK,TX,RX,COL,100,10,FDX**
- **User programmable Interrupt pin**
- **64-Pin TQFP (JEDEC LQFP) package**
- **Single 3.3 V ± 0.3V Supply**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

GENERAL

Power Management

The 78Q2120-64CGT has three power saving modes:

- Chip Power-Down
- Receive Power Management
- Transmit High Impedance Mode

Chip power-down is activated by setting the PWRDN bit in the MII register (MR0.11) or pulling high the PWRDN pin. When the chip is in power-down mode, all on-chip circuitry is shut off, and the device consumes minimum power. While in power-down state, the 78Q2120-64CGT still responds to management transactions.

Receive power management (RXCC mode) is activated by setting the RXCC bit in the MII register (MR16.0). In this mode of operation, the adaptive equalizer, the clock recovery phase lock loop (PLL), and all other receive circuitry will be powered down when no valid signal is present at the UTP receive line interface. As soon as a valid signal is detected, all circuits will automatically be powered up to resume normal operation. During this mode of operation, RX_CLK will be inactive when there is no data being received. Note that the RXCC mode is not supported during 10BASE-T operation.

Transmit high impedance mode is activated by setting the TXHIM bit in the MII register (MR16.12). In this mode of operation, the transmit UTP drivers are in a high impedance state and TXCLK is tri-stated. A weak internal pull-up is enabled on TXCLK. The receive circuitry remains fully operational. The default state of MR16.12 is a logic low for disabling the transmit high impedance mode. Only a reset condition will automatically clear MR16.12. The transmitter is fully functional when MR16.12 is cleared.

Analog Biasing

The 78Q2120-64CGT uses the reference clock and an external resistor to generate accurate bias voltages for the chip.

Clock Selection

The 78Q2120-64CGT will default to use the on-chip crystal oscillator. In this mode a 25MHz crystal is connected between the XTLP and XTLN pins. The CKIN pin should be tied low. Alternatively, an externally generated 25MHz clock can be connected to the CKIN pin. The chip senses activity on the CKIN pin, and will automatically configure itself to use the external clock. In this mode of operation, a crystal is not required and the XTLP and XTLN pins should be connected together.

Transmit Clock Generation

The transmitter uses an on-chip frequency synthesizer to generate the transmit clock. In 100BASE-TX operation, the synthesizer multiplies the reference clock by 5 to obtain the internal 125MHz serial transmit clock. In 10BASE-T mode, it generates an internal 20MHz transmit clock by multiplying the reference 25MHz clock by 4/5. The synthesizer references either the local 25 MHz crystal oscillator, or the externally applied clock, depending on the selected mode of operation.

Receive Signal Qualification

The integrated signal qualifier has separate squelch and un-squelch thresholds, and includes a built-in timer to ensure fast and accurate signal detection and receive noise rejection. Upon detection of two or more valid 10BASE-T or 100BASE-TX pulses on the line receive port, the *pass* indication, indicating the presence of valid receive signals or data will be asserted. When *pass* is asserted, the signal detect threshold is lowered by about 60%, and all adaptive circuits are released from their quiescent operating conditions, allowing them to lock onto the incoming data. In 100BASE-TX operation, *pass* will be de-asserted when no signal is presented for a period of about 1.2us. In 10BASE-T operation, *pass* will be de-asserted whenever no Manchester data is received. In either case, the signal detect threshold will return to the squelched level whenever the *pass* indication is de-asserted. The *pass* signal is used internally to control the operation of the receive clock recovery.

Receive Clock Recovery

In 100BASE-TX mode, the 125MHz receive clock is extracted using a narrow-band PLL. When no receive signal is present, the PLL is directed to lock onto the transmit 125 MHz clock. When *pass* is asserted, the PLL will use the received NRZI signal as the clock reference. The recovered clock is used to re-time the data signal and for conversion of the data to NRZ format.

In 10BASE-T mode, the 10MHz clock is recovered using a PLL. For fast acquisition, the receive PLL is locked onto the transmit reference clock during idle

receive periods. When Manchester-coded preambles are detected, the PLL adjusts its phase and re-synchronizes with the incoming Manchester data.

100BASE-TX OPERATION

100BASE-TX Transmit

The 78Q2120-64CGT contains all of the necessary circuitry to convert the transmit MII signaling from a MAC to an IEEE-802.3 compliant data-stream driving Cat-5 UTP cabling. The internal PCS interface maps 4 bit nibbles from the MII to 5 bit code groups as defined in table 24-1 of IEEE-802.3. These 5 bit code groups are then scrambled and converted to a serial stream before being sent to the MLT-3 pulse shaping circuitry and line driver. The pulse-shaper uses current modulation to produce the desired output waveform. Controlled rise/fall time in MLT-3 signal is achieved using an accurately controlled C/I filter. The line driver requires an external 1:1 isolation transformer to interface with the line media. The center-tap of the primary side of the transformer should be connected to Vcc.

100BASE-TX Receive

The 78Q2120-64CGT receives a 125MBaud MLT-3 signal through a 1:1 transformer. The signal then goes through a combination of adaptive offset adjustment (baseline wander correction) and adaptive equalization. The effect of these circuits is to sense the amount of dispersion and attenuation caused by the cable and transformer, and restore the received pulses to logic levels. The amount of gain and equalization applied to the pulses varies with the detected attenuation and dispersion and, therefore, with the length of the cable. The 78Q2120-64CGT can recover up to a 10dB of loss in signal amplitude at 16 MHz. This loss is represented as test-chan 5 in Annex A of the ANSI X3.263:199X specification and corresponds to approximately 140m of Cat5 UTP cabling. The equalized MLT-3 data signal is sliced and the resulting bit-stream is presented to the clock recovery PLL and to a serial to parallel converter. The parallel data from the converter is then descrambled and aligned into 5 bit code groups. The receive PCS interface maps these code groups to 4 bit data for the MII as outlined in table 24-1 in Clause 24 of IEEE-802.3.

PCS Bypass mode

The PCS Bypass mode is entered by pulling PCSBP high or by setting register bit MR 16.1. In this mode the 78Q2120-64CGT accepts scrambled 5 bit code into the pins TX_ER and TXD[3:0]. TX_ER is the MSB data input. The 5 bit code groups are converted to an MLT-3 signal.

The received MLT-3 signal is converted to 5 bit NRZ code groups and output from the RX_ER and RXD[3:0] pins. The RX_ER pin is the MSB data output. The RX_DV and TX_EN pins are unused in PCS Bypass mode.

10BASE-T OPERATION

10BASE-T Transmit

The 78Q2120-64CGT takes 4 bit parallel NRZ data via the MII interface and passes it through a parallel to serial converter. The data is then passed through a Manchester encoder and then on to the twisted pair pulse shaping circuitry and the twisted pair drive circuitry. An advanced pulse shaper employs a Gm-C filter to pre-distort the output waveform to meet the output voltage template and spectral content requirements detailed in Clause 14 of IEEE-802.3. Interface to the twisted pair media is through two external 50 ohm resistors and a center-tapped 1:1 transformer; no external filtering is required. During auto-negotiation and during 10BASE-T idle periods, link pulses are transmitted.

The 78Q2120-64CGT employs an onboard timer to prevent the MAC from capturing a network through excessively long transmissions. When this timer is exceeded the chip enters the jabber state, and transmission is disabled. The jabber state is exited after the MII goes idle for 500ms $\pm$ 250ms.

10BASE-T Receive

The 78Q2120-64CGT receives Manchester encoded 10BASE-T data through the twisted pair inputs and re-establishes logic levels through a slicer with a smart squelch function. The slicer automatically adjusts its level after valid data with the appropriate levels are detected. Data is passed on to the 10BASE-T PLL where the clock is recovered, data is re-timed and passed through a Manchester decoder. From here data enters the serial to parallel converter for transmission to the MAC via the media independent interface. Interface to the twisted pair media is through an external 100 ohm resistor and a 1:1 center-tapped transformer; no external filtering is required. Polarity information is detected and corrected in the internal circuitry.

Polarity Correction

The 78Q2120-64CGT is capable of either automatic or manual polarity reversal for 10BASE-T and auto-negotiation. These features are controlled by register bits MR16.5 and MR16.4. The default is automatic mode where MR16.5 is low and MR16.4 indicates if the detection circuitry has inverted the input signal. To enter manual mode, MR16.5 is set high and MR16.4 will then control the signal polarity.

SQE TEST

The 78Q2120-64CGT supports the signal quality error (SQE) function detailed in IEEE-802.3. At an interval of 1μs after each negative transition of the TXEN pin in 10BASE-T mode, the COL pin will go high for a period of 1μs. This function can be disabled through register bit MR16.11.

Natural Loopback

When enabled, and the 78Q2120-64CGT is transmitting and not receiving on the twisted pair media (10BASE-T Half Duplex mode), data on the TXD pins is looped back onto the RXD pins. During a collision, data from the RXI pins is routed to the RXD pins. The natural loopback function is enabled through register bit MR16.10.

Repeater Mode

When the RPTR pin is high or register bit MR 16.15 is set the 78Q2120-64CGT is placed in repeater mode. In this mode, full duplex operation is prohibited, CRS responds only to receive activity and, in 10BASE-T mode, the SQE test function is disabled.

AUTO-NEGOTIATION

The 78Q2120-64CGT supports the auto-negotiation functions of Clause 28 of IEEE-802.3. This function can be enabled via a pin strap to the device or through registers. If the ANEGA pin is tied high, the auto-negotiation function defaults to on and bit MR0.12, ANEGEN, is high after reset. Software can disable the auto-negotiation function by writing to bit MR0.12 If the ANEGA pin is tied low the function defaults to off and bit MR0.12 is set low after reset and cannot be written to.

The contents of register MR4 are sent to the 78Q2120-64CGT's link partner during auto-negotiation, coded in fast link pulses. Bits MR4.8:5 reflect the state of the TECH[2:0] pins after reset. If TECH[2:0] = 111, then all 4 bits are high. If TECH[2:0] = 001, then only bit 5 is high. After reset, software can change any of these bits from a 1 to a 0; but not from a 0 to a 1. Therefore, a technology permitted by the setting of the TECH pins can be disabled, but one not permitted cannot be enabled.

With auto-negotiation enabled, the 78Q2120-64CGT will start sending fast link pulses at power on, loss of link or a command to restart. At the same time it will look for either 10BASE-T idle, 100BASE-TX idle or fast link pulses from its link partner. If either idle pattern is detected, the 78Q2120-64CGT configures itself in half-duplex mode at the appropriate speed. If it detects fast link pulses, it decodes and analyzes the link code transmitted by the link partner. When three identical link code words are received (ignoring the acknowledge bit) the link code word is stored in register 5. Upon receiving three more identical link code words, with the acknowledge bit set, the 78Q2120-64CGT configures itself to the highest priority technology common to the two link partners. The technology priorities are, in descending order:

100BASE-TX, Full Duplex
100BASE-TX, Half Duplex
10BASE-T, Full Duplex
10BASE-T, Half Duplex

Once auto-negotiation is complete, register bits MR18.11:10 will reflect the actual speed and duplex that was chosen.

If auto-negotiation fails to establish a link for any reason, register bit MR18.12 will reflect this and auto negotiation will restart from the beginning. Writing a one to bit MR0.9, RANEG, will also cause auto-negotiation to restart.

MEDIA INDEPENDENT INTERFACE

MII Transmit and Receive Operation

The MII interface on the 78Q2120-64CGT provides independent transmit and receive paths for both 10Mb/s and 100Mb/s data rates as described in Clause 22 of the IEEE-802.3 standard.

The transmit clock, TX_CLK, provides the timing reference for the transfer of TX_EN, TXD[3:0], and TX_ER signals from the MAC to the 78Q2120-64CGT. TXD[3:0] is captured on the rising edge of TX_CLK when TX_EN is asserted. TX_ER is also captured on the rising edge of TX_CLK and is asserted by the MAC to request that an error code group be transmitted. The assertion of TX_ER has no affect when the 78Q2120-64CGT is operating in 10BASE-T mode.

The receive clock, RX_CLK, provides the timing reference to transfer RX_DV, RXD[3:0], and RX_ER signals from the 78Q2120-64CGT to the MAC. RX_DV transitions synchronously with respect to RX_CLK and is asserted when the 78Q2120-64CGT is presenting valid data on RXD[3:0]. RX_ER is asserted when a code group violation has been detected in the current receive packet and is also synchronous to RX_CLK.

Station Management Interface

The station management interface consists of circuitry which implements the serial protocol as described in Clause 22.2.4.4 of IEEE-802.3. A 16-bit shift register receives serial data applied to the MDIO pin at the rising edge of the MDC clock signal. Once the preamble is received, the station management control logic looks for the start-of-frame sequence and a read or write op-code, followed by the PHYAD and REGAD fields. For a read operation, the MDIO port becomes enabled as an output and the register data is loaded into a shift register for transmission. The 78Q2120-64CGT can work with a one bit preamble rather than the 32 bits proscribed by IEEE-802.3. This allows for faster programming of the registers. If a register does not exist at an address indicated by the REGAD field or if the PHYAD field does not match the 78Q2120-64CGT PHYAD indicated by the PHYAD pins, a read of the MDIO port will return all ones. For a write operation, the data is shifted in and loaded into the appropriate register after the sixteenth data bit has been received. Writes to registers not supported by the 78Q2120-64CGT are ignored.

When the PHYAD field is all zeros, the Station Management Entity (STA) is requesting a broadcast data transaction. All PHYs sharing the same Management Interface must respond to this broadcast request. All 78Q2120-64CGT will respond to the broadcast data transaction.

ADDITIONAL FEATURES

LED Indicators

There are seven LED pins that can be used to indicate various states of operation of the 78Q2120-64CGT. There is an LED pin that indicates the link is up ($\overline{\text{LEDL}}$), others that indicates the 78Q2120-64CGT is either transmitting ($\overline{\text{LEDTX}}$) or receiving ($\overline{\text{LEDRX}}$), one that signals a collision event ($\overline{\text{LEDCOL}}$), two more that reflect the data rate ($\overline{\text{LEDBTX}}$ and $\overline{\text{LEDBT}}$), and one that reflects full duplex mode of operation ($\overline{\text{LEDFDX}}$).

Interrupt Pin

The 78Q2120-64CGT has an Interrupt pin (INTR) that is asserted whenever any of the eight interrupt bits of MR17.7:0 are set. These interrupt bits can be disabled via MR17.15:8 Interrupt Enable bits. The active level of the INTR pin is controlled by the Interrupt Level bit, MR16.14. When the INTR pin is not asserted, the pin is held in a high impedance state.

PIN DESCRIPTION

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
A	Analog Pin	I	Digital Input
O	Digital Output	I/O	Digital Bi-directional Pin
S	Supply	OZ	Tri-stateable digital output

MII (MEDIA INDEPENDENT INTERFACE)

NAME	PIN	TYPE	DESCRIPTION
TX_CLK	27	OZ	TRANSMIT CLOCK: TX_CLK is a continuous clock which provides a timing reference for the TX_EN, TX_ER and TXD[3:0] signals from the MAC. The clock frequency is 25MHz in 100BASE-TX mode and 2.5MHz in 10BASE-T mode. This pin is tri-stated in isolate mode.
TX_EN	28	I	TRANSMIT ENABLE: TX_EN is asserted by the MAC to indicate that valid data for transmission is present on the TXD[3:0] pins.
TXD[3:0]	32-29	I	TRANSMIT DATA: TXD[3:0] receives data from the MAC for transmission on a nibble basis. This data is captured on the rising edge of TX_CLK when TX_EN is high.
TX_ER	26	I	TRANSMIT ERROR: TX_ER is asserted high to request that an error code-group be transmitted when TX_EN is high. In PCS bypass mode this pin becomes the higher-order bit of the transmit 5-bit code group.
CRS	34	OZ	CARRIER SENSE: When the 78Q2120-64CGT is not in repeater mode, CRS is high whenever a non-idle condition exists on either the transmitter or the receiver. In repeater mode, CRS is only active when a non-idle condition exists on the receiver. This pin is tri-stated in isolate mode.
COL	33	OZ	COLLISION: COL is asserted high when a collision has been detected on the media. In 10BASE-T mode COL is also used for the SQE test function. This pin is tri-stated in isolate mode.
RX_CLK	24	OZ	RECEIVE CLOCK: RX_CLK is a continuous clock which provides a timing reference to the MAC for the RX_DV, RX_ER and RXD[3:0] signals. The clock frequency is 25MHz in 100BASE-TX mode and 2.5MHz in 10BASE-T mode. To reduce power consumption, in 100BASE-TX mode, the 78Q2120-64CGT provides an optional mode enabled through MR16.0 in which RX_CLK is held inactive (low) when no receive data is detected. This pin is tri-stated in isolate mode.
RX_DV	23	OZ	RECEIVE DATA VALID: RX_DV is asserted high to indicate that valid data is present on the RXD[3:0] pins. In 100BASE-TX mode, it transitions high with the first nibble of preamble and is pulled low when the last data nibble has been received. In 10BASE-T mode it transitions high when the start-of-frame delimiter (SFD) is detected. This pin is tri-stated in isolate mode.
RXD[3:0]	19-22	OZ	RECEIVE DATA: Received data is provided to the MAC via RXD[3:0]. These pins are tri-stated in isolate mode.
RX_ER	25	OZ	RECEIVE ERROR: RX_ER is asserted high when an error is detected during frame reception. In PCS bypass mode this pin becomes the higher-order bit of the receive 5-bit code group. This pin is tri-stated in isolate mode.

MII (continued)

NAME	PIN	TYPE	DESCRIPTION
MDC	18	I	MANAGEMENT DATA CLOCK: MDC is the clock used for transferring data via the MDIO pin.
MDIO	17	I/O	MANAGEMENT DATA INPUT/OUTPUT: MDIO is a bi-directional port used to access management registers within the 78Q2120-64CGT. This pin requires an external pull-up resistor as specified in IEEE-802.3.

PHY ADDRESS

NAME	PIN	TYPE	DESCRIPTION
PHYAD[4:0]	12-16	I	PHY ADDRESS: Allows 31 configurable PHY addresses. The 78Q2120-64CGT always responds to data transactions via the MII interface when the PHYAD bits are all zero independent of the logic levels of the PHYAD pins.

PMA (PHYSICAL MEDIA ATTACHMENT) INTERFACE

NAME	PIN	TYPE	DESCRIPTION
PCSBP	64	I	PCS BYPASS: When high, the 100BASE-TX PCS is bypassed, as well as the scrambler and descrambler functions. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD[3:0] pins and received on the RX_ER, RXD[3:0] pins. The RX_DV and TX_EN signals are not valid in this mode. PCS bypass mode is only valid when 100BASE-TX is enabled. This mode can also be entered with MR16.1.

CONTROL AND STATUS

NAME	PIN	TYPE	DESCRIPTION
RST	6	I	RESET: When pulled low the pin resets the chip. The reset pulse must be long enough to guarantee stabilization of Vcc and startup of the oscillator. There are 2 other ways to reset the chip: i) through the internal power-on-reset (activated when the chip is being powered up) ii) through the MII register bit (MR 0.15)
PWRDN	7	I	POWER-DOWN: The 78Q2120-64CGT may be placed in a low power consumption state by setting this signal to logic high. While in power-down state, the 78Q2120-64CGT still responds to management transactions. The same power-down state can also be achieved through the PWRDN bit in the MII register (MR0.11).
ISO	2	I	ISOLATE: When set to logic one, the 78Q2120-64CGT will present a high impedance on its MII output pins. This allows for multiple chips to be attached to the same MII interface. When the 78Q2120-64CGT is isolated, it still responds to management transactions. The same high impedance state can also be achieved through the ISO bit in the MII register (MR0.10).
ISODEF	1	I	ISOLATE DEFAULT: This pin determines the power-up/reset default of the ISO bit (MR0.10). If it is connected to Vcc (GND), ISO bit will have a default value of 1 (0). When this signal is tied to Vcc, it allows multiple chips to be connected to the same MII interface.

CONTROL AND STATUS (continued)

NAME	PIN	TYPE	DESCRIPTION
ANEGA	47	I	AUTO-NEGOTIATION ABILITY: Strapped to logic high to allow auto-negotiation function. When strapped to logic low, auto-negotiation logic is disabled and manual technology selection is done through TECH[2:0]. This pin is reflected as ANEGA bit (MR1.3).
TECH[2:0]	44-46	I	TECHNOLOGY ABILITY/SELECT: TECH[2:0] sets the technology ability of the chip which is reflected in MR0.13,8 MR1.14:11 and MR4.12:5. TECH[2:0] — Technology ability 111 — Both 10BASE-T and 100BASE-TX, Both half and full duplex 001 — 10BASE-T, half duplex 010 — 100BASE-TX, half duplex 011 — Both 10BASE-T and 100BASE-TX,half duplex 100 — None 101 — 10BASE-T Both half and full duplex 110 — 100BASE-TX Both half and full duplex
RPTR	50	I	REPEATER MODE: When pulled high, this pin puts the chip into repeater mode. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10BASE-T mode, the SQE test function is disabled. This mode can also be entered with MR16.15

MDI (MEDIA DEPENDENT INTERFACE)

NAME	PIN	TYPE	DESCRIPTION
TXOP, TXON	61, 62	A	TRANSMIT OUTPUT POSITIVE/NEGATIVE: Transmitter outputs for both 10BASE-T and 100BASE-TX.
RXIP, RXIN	52, 51	A	RECEIVE INPUT POSITIVE/NEGATIVE: Receiver inputs for both 10BASE-T and 100BASE-TX.

LED INDICATORS

The LED pins use standard logic drivers. They output a logic low when the LED is meant to be on and a logic high when it is meant to be off. The LED should be connected in series with a resistor between the output pin and the power supply.

NAME	PIN	TYPE	DESCRIPTION
LEDL	40	O	LED LINK: ON for link up.
LEDTX	39	O	LED TRANSMIT: ON when there is a transmission (normally OFF).
LEDRX	38	O	LED RECEIVE: ON when there is a reception (normally OFF).
LEDCOL	37	O	LED COLLISION: In half duplex mode, this is a collision indicator and turns-ON when a collision occurs. In full duplex mode, this LED is held OFF.
LEDBTX	36	O	LED 100BASE-TX: ON for 100BASE-TX connection and OFF for other connections. $\overline{\text{LEDBTX}}$ is OFF during auto-negotiation.
LEDBT	48	O	LED 10BASE-T: ON for 10BASE-T connection and OFF for other connections. $\overline{\text{LEDBT}}$ is OFF during auto-negotiation.
LEDFDX	49	O	LED FULL DUPLEX: ON when in full duplex mode and OFF when in half duplex mode.

OSCILLATOR/CLOCK

NAME	PIN	TYPE	DESCRIPTION
CKIN	4	I	CLOCK INPUT: Connects to a 25 MHz clock source. This pin should be held low when XTLP and XTLN are being used as the 25 MHz clock source.
XTLP, XTLN	59, 58	A	CRYSTAL PINS: Should be connected to a 25 MHz crystal. When CKIN is being used as the 25 MHz clock source, these pins should be connected together.

MISCELLANEOUS PIN

NAME	PIN	TYPE	DESCRIPTION
INTR	35	OZ	INTERRUPT PIN: This pin is used to signal an interrupt to the media access controller. The pin is held in the high impedance state when an interrupt is not indicated. The pin will be forced high or low to signal an interrupt depending upon the value of the INTR_LEVEL bit (MR16.14). The events which trigger an interrupt can be programmed via the Interrupt Control Register located at address MR17.

POWER SUPPLY

NAME	PIN	TYPE	DESCRIPTION
V_{CC}	8, 11, 41, 43, 57, 63	S	SUPPLY VOLTAGE: 3.3V
GND	3, 5, 9, 10, 42, 53, 55, 60	S	GROUND

REFERENCE PIN

NAME	PIN	TYPE	DESCRIPTION
RIBB	56	A	BIAS CURRENT SETTING RESISTOR: To be tied to an external resistor which is also connected to RIBB_RET pin. This resistor should be placed as close as possible to the package pins. Suggested value is 9.76K 1%.
RIBB_RET	54	A	BIAS CURRENT SETTING RESISTOR RETURN PIN: To be connected to external RIBB resistor.

REGISTER DESCRIPTION

The 78Q2120-64CGT implements ten 16-bit registers, which are accessible via the MDIO and MDC pins. The supported registers are shown below. Unsupported registers will be read as all zeros. All of the registers respond to the broadcast address, PHYAD value 00000.

The MII management 16-bit register set implemented in the 78Q2120-64CGT is as follows:

ADDRESS	SYMBOL	NAME	RESET VALUE (HEX)
0	MR0	Control	(3100)
1	MR1	Status	(7809)
2	MR2	PHY Identifier 1	0300
3	MR3	PHY Identifier 2	(E542)
4	MR4	Auto-Negotiation Advertisement	(01E1)
5	MR5	Auto-Negotiation Link Partner Ability	0000
6	MR6	Auto-Negotiation Expansion	0000
7	MR7	(Not implemented, read as zero)	0000
8-15	MR8-15	(Reserved, read as zero)	0000
16	MR16	Vendor Specific	0540
17	MR17	Interrupt Control/Status Register	0000
18	MR18	Diagnostic Register	(0000)

Note: MR 3.3:0 contains revision specific data.

LEGEND

TYPE	DESCRIPTION	TYPE	DESCRIPTION
R	Readable by management	W	Write-able by management
RC	Cleared on a read operation	SC	Self clearing, write-able
0/1	Default value upon power-up or reset	(0/1)	Default value dependent on pin setting. The value in brackets indicates typical case.

MR0 - CONTROL REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
0.15	RESET	R, W, 0, SC	RESET: Setting this bit to logic one resets the entire 78Q2120-64CGT. This bit is self clearing.
0.14	LOOPBK	R, W, 0	LOOPBACK: When this bit is set, no transmission of data on the network medium occurs and any receive data on the network medium is ignored. By default, the loopback signal path will encompass as much of the 78Q2120-64CGT circuitry as possible.
0.13	SPEEDSL	R, W, (1)	SPEED SELECTION: This bit determines the speed of operation of the 78Q2120-64CGT. A logic one indicates 100BASE-TX operation and a logic zero indicates 10BASE-T. When auto-negotiation is enabled, this bit will have no effect on the 78Q2120-64CGT. At reset, this bit reflects the highest operating speed allowed by the TECH [2:0] pins. The MII can write to this bit, but the bit will change value only if the new value is allowed by the TECH [2:0] pins.
0.12	ANEGEN	R, W, (1)	AUTO-NEGOTIATION ENABLE: The auto-negotiation process is enabled by setting this bit to a logic one. This bit can only be set to logic one if the ANEGA pin is a logic one and will default to a logic one upon reset in this case. If this bit is cleared to logic zero, manual speed and duplex mode selection is accomplished through bits 0.8 (DUPLEX) and 0.13 (SPEEDSL) of the configuration register or the TECH[2:0] pins according to the table shown in the section describing the TECH[2:0] pins. If the ANEGA pin is brought from zero to one and reset is not asserted, this bit will remain at zero until a one is written.
0.11	PWRDN	R, W, 0	POWER-DOWN: The 78Q2120-64CGT may be placed in a low power consumption state by setting this bit to logic one. While in power-down state, the 78Q2120-64CGT still responds to management transactions. The power-down state can also be achieved by setting PWRDN pin high.
0.10	ISO	R, W, (0)	ISOLATE: When set, the 78Q2120-64CGT will present a high impedance on its MII output pins. This allows for multiple PHY to be attached to the same MII interface. When the 78Q2120-64CGT is isolated, it stills responds to management transactions. The default value of this bit depends on the ISODEF pin. When ISODEF pin is tied high the ISO bit defaults to high. When ISODEF pin is tied low, the ISO bit defaults to low. The same high impedance state can be achieved through the ISO pin.
0.9	RANEG	R, W, 0, SC	RESTART AUTO-NEGOTIATION: Normally, the auto-negotiation process is started at power-up. The process can be restarted by setting this bit to logic one. This bit is self clearing.

MR0 - CONTROL REGISTER (continued**)**

BIT	SYMBOL	TYPE	DESCRIPTION
0.8	DUPLEX	R, W, (1)	DUPLEX MODE: This bit determines whether the 78Q2120-64CGT supports full duplex or half duplex. A logic one indicates full duplex operation and a logic zero indicates half duplex. When auto-negotiation is enabled, this bit will have no effect on the 78Q2120-64CGT. At reset, this bit reflects the highest operating mode allowed by the TECH [2:0] pins. The MII can write to this bit, but the bit will change value only if the new value is allowed by the TECH pins.
0.7	COLT	R, W, 0	COLLISION TEST: When this bit is set to one, the 78Q2120-64CGT will assert the COL signal in response to the assertion of TX_EN signal. Collision test is disabled in PCS bypass mode. Collision test is enabled regardless of the duplex mode of operation.
0.6:0	RSVD	R, 0	RESERVED

MR1 - STATUS REGISTER

Bits 1.15 through 1.11 reflect the ability of the 78Q2120-64CGT as configured by the TECH[2:0] pins They do not reflect any ability changes made via the MII management interface to bits 0.13 (SPEEDSL), 0.12 (ANEGEN) and 0.8 (DUPLEX).

BIT	SYMBOL	TYPE	DESCRIPTION
1.15	100T4	R, 0	100BASE-T4 ABILITY: This bit is permanently held at logic zero to indicate that the 78Q2120-64CGT is not capable of 100BASE-T4.
1.14	100X_F	R, (1)	100BASE-TX FULL DUPLEX ABILITY: (0 = not able, 1 = able)
1.13	100X_H	R, (1)	100BASE-TX HALF DUPLEX ABILITY: (0 = not able, 1 = able)
1.12	10T_F	R, (1)	10BASE-T FULL DUPLEX ABILITY: (0 = not able, 1 = able)
1.11	10T_H	R, (1)	10BASE-T HALF DUPLEX ABILITY: (0 = not able, 1 = able)
1.10:6	RSVD	R, 0	RESERVED
1.5	ANEGC	R, 0	AUTO-NEGOTIATION COMPLETE: A logic one indicates a) that the auto-negotiation process has completed, b) that the contents of registers MR4, 5, and 6 are valid, and c) that a highest common denominator rate and mode have been found.
1.4	RFAULT	R, 0, RC	REMOTE FAULT: A logic one indicates that a remote fault condition has been detected. It remains set until it is cleared. This bit can only be cleared by reading this register (MR1) via the management interface.
1.3	ANEGA	R, (1)	AUTO-NEGOTIATION ABILITY: This bit, when set, indicates the ability to perform auto-negotiation. The value of this bit is determined by the ANEGA pin.
1.2	LINK	R, 0	LINK STATUS: A logic one indicates that a valid link has been established. If the link status should transition from an OK status to a NOT-OK status, this bit will become cleared and remain cleared until it is read.
1.1	JAB	R, 0, RC	JABBER DETECT: In 10Base-T mode, this bit is set during a jabber event. After a jabber event it remains set until cleared by a read operation.
1.0	EXTD	R, 1	EXTENDED CAPABILITY: This bit is permanently set to logic one to indicate that the 78Q2120-64CGT provides an extended register set (MR2 and beyond).

MR2, 3 - PHY IDENTIFIER REGISTER

2.15:0	OUI	R, 0300h	ORGANIZATIONALLY UNIQUE IDENTIFIER: This value is 00-C0-39 for TDK Semiconductor Corporation. This translates to a value of 300h for this register.
3.15:10	OUI	R, 111001	ORGANIZATIONALLY UNIQUE IDENTIFIER: Remaining 6 bits of the OUI.
3.9:4	MN	R, 010100	MODEL NUMBER: The last 2 digits of the model number 78Q2120-64CGT is encoded into the 6 bits. (20d = 14h)
3.3:0	RN	R	REVISION NUMBER: For example, a value of 0010 corresponds to the second version of the silicon.

MR4 - AUTO-NEGOTIATION ADVERTISEMENT REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
4.15	NP	R,0	NEXT PAGE: Not supported; permanently tied to logic zero.
4.14	RSVD	R,0	RESERVED: This bit is permanently set to logic 0.
4.13	RF	R, W, 0	REMOTE FAULT: When internally set to logic one, the MII management interface indicates to the link partner a remote fault condition.
4.12:5	TAF	R, W, (0Fh)	TECHNOLOGY ABILITY FIELD: The default value of this field is dependent upon MR1.15:11 bits. This field can be overwritten by management to auto-negotiate to an alternate common technology. Writing to this register has no effect until auto-negotiation is enabled.
4.12:10	A7:5	R, 000	Reserved for future technology.
4.9	A4	R, 0	100BASE-T4: The 78Q2120-64CGT does support 100BASE-T4.
4.8	A3	R, W, (1)	100BASE-TX FULL DUPLEX: The default value of this bit follows MR1.14 bit. When the default is zero, this bit set by the management.
4.7	A2	R, W, (1)	100BASE-TX:The default value of this bit follows MR 1.13 bit. When the default is zero, this bit cannot be set by the management.
4.6	A1	R, W, (1)	10BASE-T FULL DUPLEX: The default value of this bit follows MR1.12 bit. When the default is zero, this bit cannot be set by the management.
4.5	A0	R, W, (1)	10BASE-T: The default value of this bit follows MR1.11 bit. When the default is zero, this bit cannot be set by the management.
4.4:0	S4:0	R, 00001	SELECTOR FIELD: Hard coded with the value of 00001 for IEEE-802.3.

MR5 - AUTO-NEGOTIATION LINK PARTNER ABILITY REGISTER

5.15	NP	R, 0	NEXT PAGE: When set, it indicates that the link partner wishes to engage in next page exchange.
5.14	ACK	R, 0	ACKNOWLEDGE: When set, it indicates that the link partner has successfully received at least 3 consecutive and consistent FLP bursts.
5.13	RF	R, 0	REMOTE FAULT: When set, it indicates that the link partner has a fault.
5.12:5	A7:0	R, 0	TECHNOLOGY ABILITY FIELD: This field contains the technology ability of the link partner. The bit definition is the same as MR4.12:5.
5.4:0	S4:0	R, 00000	SELECTOR FIELD: This field contains the type of message sent by the link partner. For IEEE-802.3 compliant link partner transceiver, this field should be 00001.

MR6 - AUTO-NEGOTIATION EXPANSION REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
6.15:5	RSVD	R, 0	RESERVED
6.4	PDF	R, 0, RC	PARALLEL DETECTION FAULT: When set, it indicates that more than one technology was detected during link up. This bit is cleared when read.
6.3	LPNPA	R, 0	LINK PARTNER NEXT PAGE ABLE: When set, it indicates that the link partner supports the next page function.
6.2	NPA	R, 0	NEXT PAGE ABLE: Permanently tied to logic zero since the 78Q2120-64CGT does not support next page function.
6.1	PRX	R, 0, RC	PAGE RECEIVED: Set when a properly matched link code word has been received into the Auto-negotiation Link Partner. This bit is cleared when read.
6.0	LPANEGA	R, 0	LINK PARTNER AUTO-NEGOTIATION ABLE: When set it indicates that the link partner is able to participate in the auto-negotiation function.

MR16 - VENDOR SPECIFIC REGISTER

16.15	RPTR	R, W, (0)	REPEATER MODE: When set, this bit puts the chip into repeater mode. In this mode, full duplex is prohibited, CRS responds to receive activity only and, in 10BASE-T mode, the SQE test function is disabled.
16.14	INT LEVEL	R, W, 0	When this bit is a zero, the INTR pin is forced low to signal an interrupt. Setting this bit causes the INTR pin to be forced high to signal an interrupt.
16.13	RSVD	R, 0	RESERVED
16.12	TXHIM	R, W, 0	TRANSMIT HIGH IMPEDANCE: When this bit is set, the transmitter UTP drivers are in a high impedance state and TXCLK is tri-stated. The receive circuitry remains fully functional. Only a reset condition will automatically clear this bit.
16.11	SQE TEST INHIBIT	R, W, 0	Setting this bit disables 10BASE-T SQE testing. By default, when this bit is a zero, the SQE test is performed by generating a COL pulse following the completion of a packet transmission.
16.10	10BT NATURAL LOOPBACK	R, W, 0	Setting this bit causes transmitted data on TXD to be automatically looped back to the RXD receive signals when 10BASE-T mode is enabled.
16.9	RSVD	R, 0	RESERVED
16.8	RSVD	R, 1	RESERVED

MR16 - VENDOR SPECIFIC REGISTER (continued)

BIT	SYMBOL	TYPE	DESCRIPTION
16.7	RSVD	R, 0	RESERVED
16.6	RSVD	R, 1	RESERVED
16.5	APOL	R, W, 0	AUTO POLARITY: During auto-negotiation and 10BASE-T mode, the 78Q2120-64CGT is able to automatically invert the received signal - both the Manchester data and link pulses - if necessary. Setting this bit disables this feature.
16.4	RVSPOL	R, (W), 0	REVERSE POLARITY: The reverse polarity is detected either through 8 inverted 10BASE-T link pulses (NLP) or through one burst of inverted fast link pulses (FLP). When the reverse polarity is detected, the 78Q2120-64CGT will invert the receive data path and set this bit to logic one if the feature is not disabled. If $\overline{\text{APOL}}$ is a logic 1, then this bit is write-able. Setting this bit forces the polarity to be reversed.
16.3:2	RSVD	R,W,00	RESERVED. Must be zero.
16.1	PCSBP	R,W,0	PCS BYPASS: When set, the 100BASE-TX PCS is bypassed, as are the scrambler and descrambler functions. Scrambled 5-bit code groups for transmission are applied to the TX_ER, TXD[3:0] pins and received on the RX_ER, RXD[3:0] pins. The RX_DV and TX_EN signals are not valid in this mode. PCSBP mode is only valid when 100BASE-TX is enabled.
16.0	RXCC	R,W,0	RECEIVE CLOCK CONTROL: When set, the RX_CLK signal will be held in logic low (only in 100BASE-TX mode) when there is no data being received (to save power). The RX_CLK signal will restart 1 clock cycle before the assertion of RX_DV and be shut off 64 clock cycles after RX_DV goes low. RXCC is disabled when loopback mode is enabled (MR0.14 is high). This bit should be kept at logic zero when the chip is in PCS Bypass mode.

MR17 - INTERRUPT CONTROL/STATUS REGISTER

The Interrupt Control/Status Register provides the means for controlling and observing the events which trigger an interrupt on the INTR pin. This register can also be used in a polling mode via the MII serial interface as a means to observe key events within the PHY via one register address. These bits are cleared after the register is read. Bits 8-15 of this register, when set to logic one, enable their corresponding bit in the lower byte to signal an interrupt on the INTR pin. The level of this interrupt can be set via MR16.14.

BIT	SYMBOL	TYPE	DESCRIPTION
17.15	JABBER IE	R, W, 0	JABBER INTERRUPT ENABLE BIT
17.14	RXER IE	R, W, 0	RECEIVE ERROR INTERRUPT ENABLE BIT
17.13	PRX IE	R, W, 0	PAGE RECEIVED INTERRUPT ENABLE BIT
17.12	PFD IE	R, W, 0	PARALLEL DETECT FAULT INTERRUPT ENABLE BIT
17.11	LP-AC K IE	R, W, 0	LINK PARTNER ACKNOWLEDGE INTERRUPT ENABLE BIT
17.10	LS-CHG IE	R, W, 0	LINK STATUS CHANGE INTERRUPT ENABLE BIT
17.9	RFAULT IE	R, W, 0	REMOTE FAULT INTERRUPT ENABLE BIT
17.8	ANEG-COMP IE	R, W, 0	AUTO-NEGOTIATION COMPLETE INTERRUPT ENABLE BIT
17.7	JABBER INT	RC, 0	JABBER INTERRUPT: This bit is set when a jabber event is indicated by the 10BASE-T circuitry.
17.6	RXER INT	RC, 0	RECEIVE ERROR INTERRUPT: This bit is set when the RX_ER signal transitions high.
17.5	PRX INT	RC, 0	PAGE RECEIVE INTERRUPT: This bit is set when a new page has been received from the link partner during auto-negotiation.
17.4	PDF INT	RC, 0	PARALLEL DETECT FAULT INTERRUPT: This bit is set by the auto-negotiation logic when a parallel detect fault condition is indicated.
17.3	LP-ACK INT	RC, 0	LINK PARTNER ACKNOWLEDGE INTERRUPT: This bit is set by the auto-negotiation logic when FLP bursts are received with the acknowledge bit set.
17.2	LS-CHG INT	RC, 0	LINK STATUS CHANGE INTERRUPT: This bit is set when the link transitions from an OK status to a fail status or vice versa.
17.1	RFAULT INT	RC, 0	REMOTE FAULT INTERRUPT: This bit is set when a remote fault condition has been indicated by the link partner.
17.0	ANEG-COMP INT	RC, 0	AUTO-NEGOTIATION COMPLETE INTERRUPT: This bit is set by the auto-negotiation logic upon successful completion of auto-negotiation.

MR18 - DIAGNOSTIC REGISTER

BIT	SYMBOL	TYPE	DESCRIPTION
18.15:13	RSVD	R, 0	RESERVED
18.12	ANEGF	R,0,RC	AUTO-NEGOTIATION FAIL: This bit is set when auto-negotiation completes and no common technology was found. It remains set until read.
18.11	DPLX	R, 0	DUPLEX: This bit indicates the result of the auto-negotiation for duplex arbitration. If set it indicates that full-duplex was the highest common denominator. If clear it indicates that half-duplex was the highest common denominator.
18.10	RATE	R, 0	RATE: This bit indicates the result of the auto-negotiation for data rate arbitration. If set it indicates that 100BASE-TX was the highest common denominator. If clear it indicates that 10BASE-T was the highest common denominator.
18.9	RX-PASS	R, 0	RECEIVE PASS: In 10BASE-T mode, this bit indicates that Manchester data has been detected. In 100BASE-TX mode, it indicates that a valid received signal has been detected (but not necessarily locked on to).
18.8	RX-LOCK	R, 0	RECEIVE LOCK: Indicates that the receive PLL has locked onto the received signal for the selected speed of operation (10BASE-T or 100BASE-TX). This bit is cleared whenever a cycle-slip occurs, and will remain cleared until it is read.
18.7:0	RSVD	R, W, 0	RESERVED. Must be zero.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum rating may permanently damage the device.

PARAMETER	RATING
DC Supply Voltage	7 VDC
Storage Temperature	-65 to 150°C
Pin Voltage	-0.3 to (Vcc+0.3) VDC
Pin Current	± 100 mA

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges:

DC Voltage Supply, Vcc	3.3 V ± 0.3VDC
Ambient Operating Temperature, Ta	0 - 70°C

DC CHARATERISTICS:

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Current	I_{CC}	V_{CC} = 3.3V; Auto-Negotiation 10BT (Idle) 10BT (Normal Activity) 100BTX Transmit High Impedance		 25 25 85 95 30	 30 30 100 115 35	mA
Supply Current	I_{CC}	Powerdown mode		500	800	µA

DIGITAL INPUT CHARACTERISTICS

Pins of type I, I/O

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
TTL Input Voltage Low	V_{IL}				0.8	V
TTL Input Voltage High	V_{IH}		2.0			V
TTL Input Current	I_{IL}, I_{IH}	V_{CC} = 3.3V	-10		+10	µA
Input Capacitance	C_{IN}			10		pF

DIGITAL OUTPUT CHARACTERISTICS

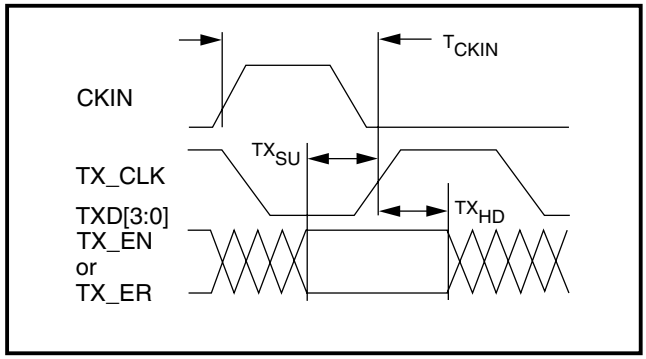
Pins of type O, I/O, OZ

Output Voltage High	V_{OH}	$3.0V \le V_{CC} \le 3.6V$ I_{OH} = 2.0mA	V_{CC}-0.4			V
Output Voltage Low	V_{OL}	$3.0V \le V_{CC} \le 3.6V$ I_{OL} = 2.0mA			0.4	V
Output Transition Time Between V_{OL} and V_{OH}	T_t	$3.0V \le V_{CC} \le 3.6V$ I_{OH}, I_{OL} = 2.0mA		5		ns

DIGITAL TIMING CHARACTERISTICS

MII Transmit Interface

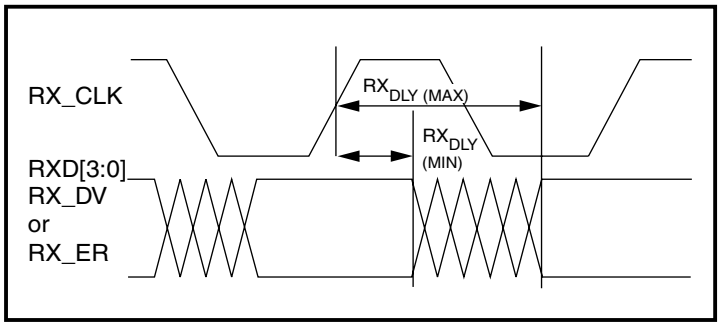
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{SU}		15			ns
Hold Time: TX_CLK to TXD[3:0], TX_EN, TX_ER	TX_{HD}		0			ns
CKIN-to-TX_CLK Delay	T_{CKIN}		20		35	ns
TX_CLK Duty-Cycle			40		60	%



Transmit Inputs to the 78Q2120-64CGT

MII Receive Interface

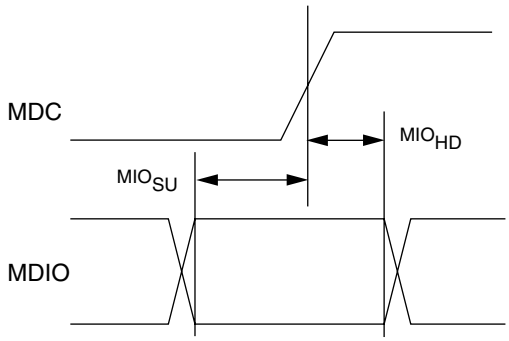
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Receive Output Delay: RX_CLK to RXD[3:0], RX_DV, RX_ER	RX_{DLY}		10		30	ns
RX_CLK Duty-Cycle			40		60	%



Receive Outputs from the 78Q2120-64CGT

MDIO Interface Input Timing

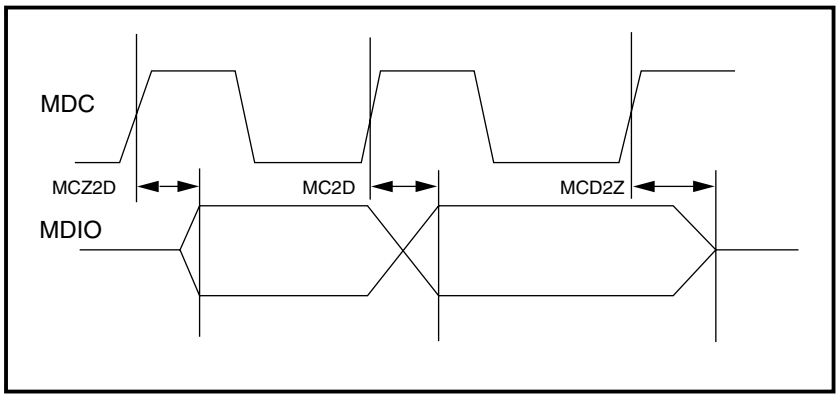
CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Setup Time: MDC to MDIO	MIO_{SU}		10			ns
Hold Time: MDC to MDIO	MIO_{HD}		0			ns
Max Frequency: MDC	F_{max}				25	MHz



MDIO as an Input to the 78Q2120-64CGT

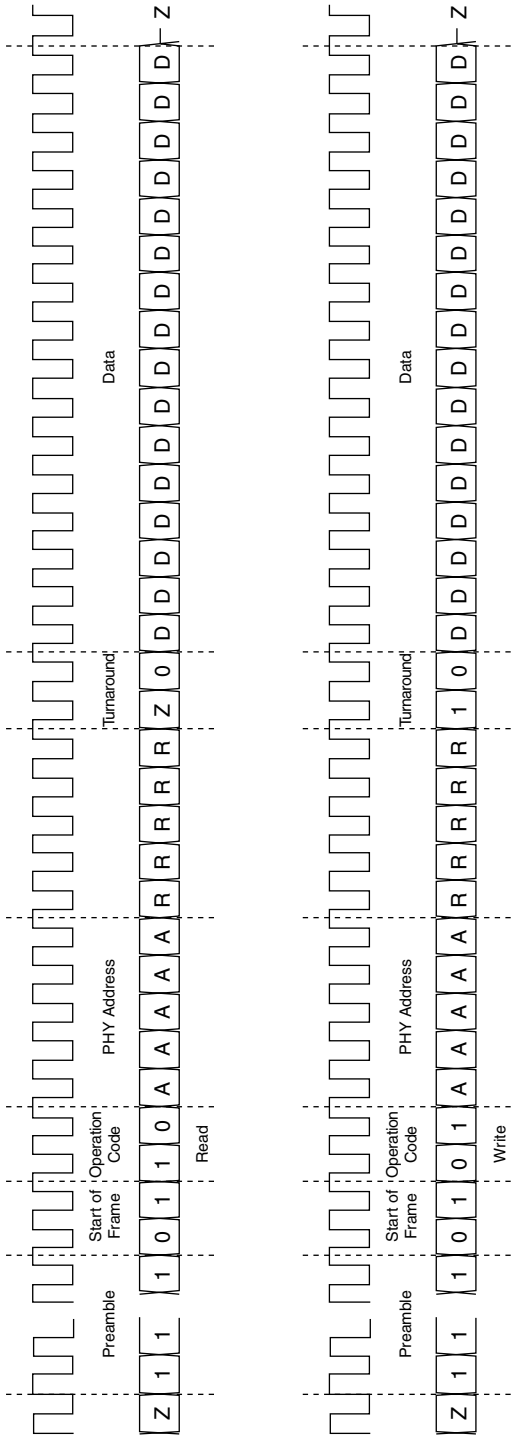
MDIO Interface Output Timing

CHARACTERISTICS	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
MDC to MDIO data delay	MC2D				30	ns
MDIO output from high Z to driven after MDC	MCZ2D				30	ns
MDIO output from driven to high Z after MDC	MCD2Z				30	ns



MDIO as an Output from the 78Q2120-64CGT

MDIO Interface Output Timing



100BASE-TX System Timing

System timing requirements for 100BASE-TX operation are listed in table 24-2 of Clause 24 of IEEE 802.3.

PARAMETER	CONDITION	NOM	UNIT
TX_EN Sampled to first bit of “J” on MDI output		12	BT
First bit of “J” on MDI input to CRS assert		15	BT
First bit of “T” on MDI input to CRS de-assert		23	BT
First bit of “J” on MDI input to COL assert		16	BT
First bit of “T” on MDI input to COL de-assert		24	BT
TX_EN Sampled to CRS assert	RPTR = low	4	BT
TX_EN sampled to CRS de-assert	RPTR = low	4	BT

10BASE-T System Timing

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
TX_EN (MII) to TD Delay				6	BT
RD to RXDat (MII) Delay				6	BT
Collision delay				9	BT
SQE test wait			1		µs
SQE test duration			1		µs
Jabber on-time*		20		150	ms
Jabber off-time*		250		750	ms

***** Guarantee by design. The specifications in the following table are included for information only.

ANALOG ELECTRICAL CHARACTERISTICS

100BASE-TX Transmitter

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Output Amplitude, Vp+, Vp- (See note below)	Best-fit over 14 bit times; 0.5 dB Transformer loss	950		1050	mV
Output Amplitude Symmetry	$\frac{\lvert Vp+\rvert}{\lvert Vp-\rvert}$	0.98		1.02	
Output Overshoot	Percent of Vp+, Vp-			5	%
Rise/Fall time, tr, tf	10 - 90% of Vp+, Vp-	3		5	ns
Rise/Fall time Imbalance	$\lvert tr - tf \rvert$			500	ps
Duty Cycle Distortion	Deviation from best-fit time-grid; 010101... Sequence			±250	ps

100BASE-TX Transmitter

The specifications in the following table are included for information only.

PARAMETER	CONDITION	MIN	MAX	UNIT
Return Loss	2 < f < 30 MHz 30 < f < 60 MHz 60 < f < 80 MHz	16 $16 - 20\log\left(\frac{f}{30MHz}\right)$ 10		dB
Open Circuit Inductance	-8 < Iin < 8 mA	350		µH
Jitter	Scrambled Idle		1.4	ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103
Line Termination: 100Ω ±1%
RIBB: 9.76k ±1% @ 3.3V

The specifications in the following table are included for information only.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Signal Detect Assertion Threshold (pk-pk)		600	900	1000	mV
Signal Detect De-assertion Threshold (pk-pk)		300	350	400	mV
Differential Input Resistance		20			kΩ
PLL Locking Time			5		µs
Jitter Tolerance (pk-pk)			4		ns
Baseline Wander Tracking		-75		+75	%
Signal Detect Assertion Time				200	µs
Signal Detect De-assertion Time				1.4	µs

10BASE-T Transmitter

The Manchester-encoded data pulses, the link pulse and the start-of-idle pulse are tested against the templates and using the procedures found in Clause 14 of IEEE 802.3.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Peak Differential Output Signal (see note)	All data patterns	2.2		2.8	V
Link Pulse Width			100		ns
Start-of-Idle Pulse Width		300		350	ns

Note: Measured at the line side of the transformer.

Test Condition: Transformer P/N: TLA-6T103

Line Termination: 100Ω ±1%

RIBB: 9.76k ±1% @ 3.3V

10BASE-T Transmitter

The specifications in the following table are included for information only.

Output return loss		15			dB
Harmonic Content	Any harmonic; dB below fundamental; All ones data	27			dB
Output Impedance Balance	1 MHz < freq < 20 MHz	$29 - 17\log\left(\frac{f}{10}\right)$			dB
Peak Common-mode Output Voltage				50	mV
Common-mode rejection	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			100	mV
Common-mode rejection jitter	15 V_{pk}, 10.1 MHz sine wave applied to transmitter common-mode. All data sequences.			1	ns

10BASE-T Receiver

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
PLL Locking Time			1.8		µs
Jitter Tolerance (pk-pk)			32		ns
Input Squelched Threshold		600	900	1000	mV
Input Un-squelch Threshold		300	350	400	mV

10BASE-T Receiver

The specifications in the following table are included for information only.

Bit Error Ratio			10^{-10}		
Differential Input Resistance		20			kΩ
Common-mode rejection	Square wave 0 < f < 500 kHz	25			V

ISOLATION TRANSFORMERS

Two simple 1:1 isolation transformers are all that are required at the line interface, but transformers with integrated common-mode choke are recommended for exceeding FCC requirements. This table gives the recommended line transformer characteristics:

NAME	VALUE	CONDITION
Turns Ratio	1 CT : 1 CT ± 5%	
Open-Circuit Inductance	350 uH (min)	@ 10 mV, 10 kHz
Leakage Inductance	0.40 uH (max)	@ 1 MHz (min)
Inter-Winding Capacitance	12 pF (max)	
D.C. Resistance	0.9 Ω (max)	
Insertion Loss	1.1 dB (typ)	0 - 100 MHz
HIPOT	1500 Vrms	

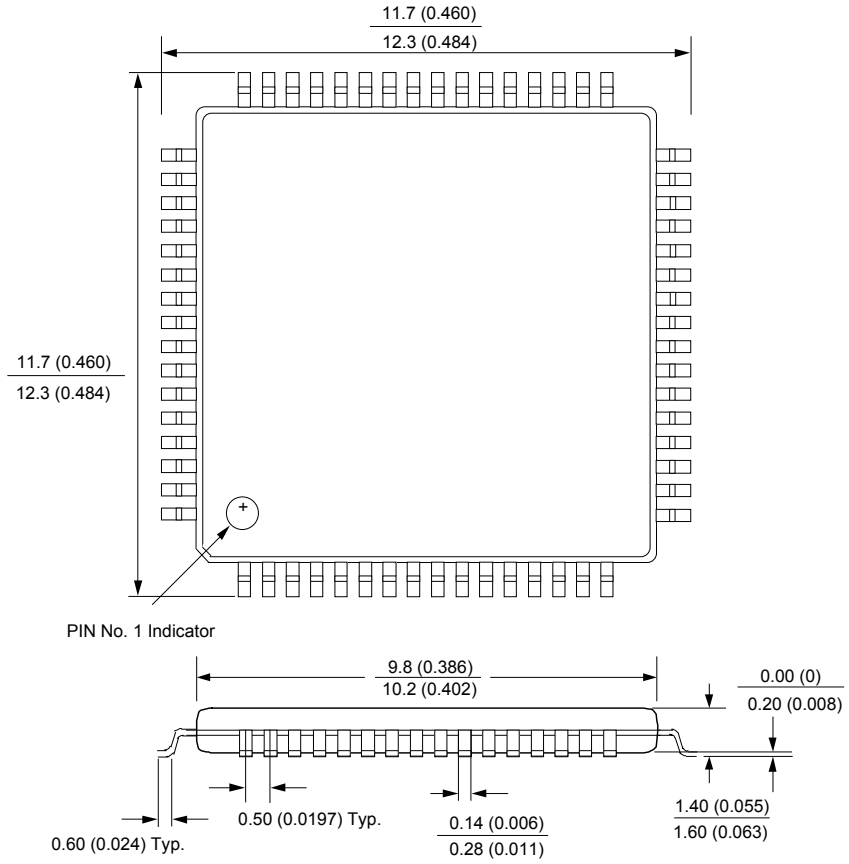
Note: The 100Base-TX amplitude specifications assume a transformer loss of 0.5 dB. For the transmit line transformer, insertion loss up to 1.3 dB can be compensated by increasing the line drive current by means of reducing the RIBB resistor value.

REFERENCE CRYSTAL

If the internal crystal oscillator is to be used, a crystal with the following characteristics should be chosen:

NAME	VALUE	UNITS
Frequency	25.00000	MHz
Load Capacitance	15	pF
Frequency Tolerance	±50	PPM
Aging	±2	PPM/yr
Temperature Stability (0 - 70°C)	±5	PPM
Oscillation Mode	Parallel Resonance, Fundamental Mode	
Parameters at 25°C ± 2°C ; Drive Level = 0.5 mW		
Shunt Capacitance (max)	8	pF
Motional Capacitance (min)	10	fF
Series Resistance (max)	25	Ω
Spurious Response (max)	> 5 dB below main within 500 kHz	

MECHANICAL DRAWING

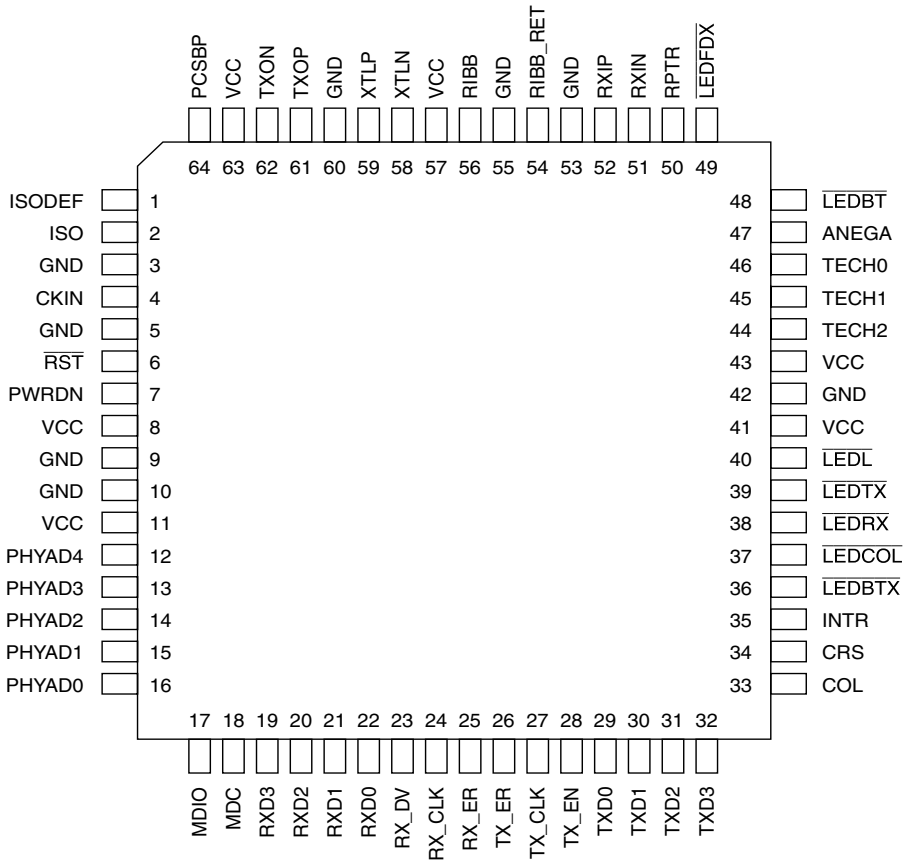


64-TQFP (JEDEC LQFP)

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component



64-Lead TQFP (JEDEC LQFP)
78Q2120-64CGT

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
78Q2120-64CGT	64-pin Plastic TQFP	78Q2120-64CGT	78Q2120-64T

TDK Semiconductor Corporation, 2642 Michelle Drive, Tustin, CA 92780-7019, (714) 508-8800, FAX: (714) 508-8877